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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/886,885	06/21/2001	Grant H. McGibney	266P004	6122

7590 06/23/2005

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Buffalo Grove, IL 60089-2073

EXAMINER

PHAN, MAN U

ART UNIT	PAPER NUMBER
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2665

DATE MAILED: 06/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/886,885

Applicant(s)

MCGIBNEY, GRANT H.

Examiner

Man Phan

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 07 April 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☐ Claim(s) _____ is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 1-15, 18 and 19 is/are allowed.
- 6) ☒ Claim(s) 16 and 17 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 21 June 2001 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☒ None of:
- 1) ☒ Certified copies of the priority documents have been received.
 - 2) ☐ Certified copies of the priority documents have been received in Application No. _____.
 - 3) ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

Response to Amendment and Argument

1. This communication is in response to applicant's 04/07/2005 Amendment in the application of McGibney for a "Centralized synchronization for wireless networks" filed 06/21/2001. This application claims foreign priority based on the application 2,347,927 filed May 16, 2001 in Canada. It is noted, however, that applicant has not filed a certified copy of the CANADA 2,347,927 application as required by 35 U.S.C. 119(b). The amendments and response have been entered and made of record. Claims 1-19 are pending in the application.
2. Applicant's remarks and argument to the rejected claims are insufficient to distinguish the claimed invention from the cited prior arts or overcome the rejection of said claims under 35 U.S.C. 103 as discussed below. Applicant's argument with respect to the pending claims have been fully considered, but they are not persuasive for at least the following reasons.
3. Applicant's argument with respect to the rejected claim 1 that the cited references fails to disclose or suggest "*vernier signal*". However, Examiner first wishes to point out the understanding of timing vernier in the synchronization. Generally several timing verniers are used to divide the period of the clock signal into several time slots. In typical, the fixed frequency clock signal is sent to all timing verniers from which all signal generation and sampling are measured to determine the time offset. As described in 1998 IEEE International Solid-State Circuits Conference (ISSCC) Vol. 34, No. 4, pp.160-161, 431, 126-127, 385, Y. Morooka et al., "Source Synchronization and Timing Vernier Techniques for 1.2 GB/s

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SLDRAM Interface" by Yasunobu Nakase et al. Apr. 1999. pp. 494-501). With that understanding and as discussed in the previous Office Action, Bortolini et al. (US#6,163,549) is applied herein merely for the teaching of the synchronization of a timing unit to an external link utilizing "*timing signals*". Bortolini teaches an apparatus and method in which local timing units synchronized to a centralized timing unit determine the difference in timing between external links and the local timing units (*determining time offset*). This difference in timing (*time offset*) is then transmitted to the central timing unit, which utilizes this information to adjust the timing of the central timing unit for the synchronization. The adjustment to the central timing unit brings it into synchronization with the selected external link (Col. 1, lines 56 plus). Furthermore, Bortolini teaches in Figs. 6 & 8 the block diagrams illustrated the timing synchronization, in which the remote phase detection is performed so that STU 601 can be locked in phase and frequency to STM-1 link 103 via port unit 117. The output of counter 805 is latched into latch 806 under control of the MFS signal received via lead 638 from *timing signal generator 604*. The MFS signal occurs every 500 microseconds and is transmitted on lead 638 of Fig. 6. The difference between latches 806 and 807 represents the number of input clock periods which occurred during the last MFS interval. An expected difference number is then used to reduce the number of bits that must be transmitted by remote phase controller 809. The expected difference number is the number of clock periods which could be expected if STU 601 is in perfect synchronization with the STM-1 link to which STU 601 is synching (See also Figs. 9-12; Col. 12, lines 2 plus). Bortolini also teach in Fig. 12 illustrates the details of digital synthesizer 1012 of Fig. 10 utilizing flip flop 1214. *The purpose of this flip flop is to synchronize the enable signal to the timing vernier with the desired trigger being use* (Col. 14, lines 50 plus). Therefore,

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examiner maintains that the references cited and applied in the last office actions for the rejection of the claims are maintained in this office action.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 16 & 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hall et al. (US#6,208,871) in view of Bortolini et al. (US#6,163,549).

With respect to claims 16, 17, Hall et al. (US#6,208,871) discloses a novel system and method for synchronizing timing in a wireless communication system, according to the essential features of the claims. Hall et al. (US#6,208,871) provides a time adjustment to a base transceiver station from a mobile station, in order to synchronize the base transceiver station to the wireless communication system reference time (Col. 3, lines 17 plus). Hall teaches in Fig. 3 a flow chart illustrated a method for providing time adjustment to wireless communication system 100, in which at block 324, random mobile station 103 determines a timing adjustment calculation based on the first time offset of the first signal from the first base transceiver station

and the second time offset of the second signal from the second base transceiver station. First, a controller in random mobile station 103 calculates a time offset difference between the first and second PN short code time offsets resulting from the identity, to form a desired time offset. The controller then calculates a difference between the first time offset and the second time offset to form a measured time offset. Finally, the controller compares the desired time offset to the measured time offset to determine a timing adjustment calculation (Col. 6, lines 24 plus).

However, Hall et al. does not expressly disclose a vernier signal generator connected to supply a vernier signal (*the main clock or time base is assumed to be stable*) to the transmitter. In the same field of endeavor, Bortolini et al. (US#6,163,549) discloses a the synchronization of a timing unit to an external link. Bortolini teaches an apparatus and method in which local timing units synchronized to a centralized timing unit determine the difference in timing between external links and the local timing units. This difference in timing is then transmitted to the central timing unit, which utilizes this information to adjust the timing of the central timing unit. Advantageously, the adjustment to the central timing unit brings it into synchronization with the selected external link. Advantageously, the local timing units are synchronized to the central timing unit via multiple timing paths set up through switching units within the network. Each switching unit switches one bit of data for each group of data being received on each of the external links. In addition, information received by each of the external links designating the accuracy of the external link is transmitted to the central timing unit so that the central timing unit can select the external link having the highest accuracy.

One skilled in the art would have recognized the need for effectively and efficiently synchronizing a base oscillator to a remote oscillator, and would have applied Bortoloni's

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synchronization of a timing unit to an external link into Hall's teaching of timing synchronization between a base oscillator and remote oscillator. Therefore, It would have been obvious to a person of ordinary skill in the art at the time of the invention was made to apply Bortolini's synchronizing a central timing unit to an external link via a switching network into Hall's method and apparatus for providing a time adjustment to a wireless communication system with the motivation being to provide a centralized synchronization for wireless networks

Allowable Subject Matter

5. Claims 1-15 and 18, 19 are allowable

6. The following is an examiner's statement of reasons for the indication of allowable subject matter: The closest prior art of record fails to disclose or suggest wherein an equalization controller connected to the pre-equalizer filter to provide radio channel corrections and a timing advance to signals transmitted from the base station and connected to the post-equalizer filter to provide radio channel corrections and a timing advance to signals received from the terminal; a synchronization controller connected to receive frame position information from the frame counter and being configured to determine a timing advance required to adjust the base oscillator to be synchronized to the remote oscillator, the synchronization controller being connected to supply the timing advance to the equalization controller; and the synchronization controller being configured to generate a vernier signal, in which the vernier signal comprises successive time

segments, each time segment being offset in time from a multiple of the remote sample period by different multiples of a fraction of the remote sample period, as expressly recited in claims.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The Bortolini (US#5,483,201) is cited to show the synchronization circuit using a high speed digital slip counter.

The Goto et al. (US#5,280,195) is cited to show the timing generator.

The Chapman et al. (US#5,684,421) is cited to show the compensated delay locked loop timing vernier.

The Coy et al. (US#5,952,949) is cited to show the timer with dynamic reset threshold.

The Mydill (US#6,243,841) is cited to show the automated test and evaluation sampling system and method.

The Akita (US#6,373,303) is cited to show the sync signal generating circuit provided in semiconductor integrated circuit..

The Choudhury (US#6,229,367) is cited to show the method and apparatus for generating a time delayed signal with a minimum data dependency error using an oscillator.

Conclusion

8. **THIS ACTION THIS ACTION IS MADE FINAL.** See MPEP ' 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to M. Phan whose telephone number is (571) 272-3149. The examiner can normally be reached on Mon - Fri from 6:00 to 3:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy Vu, can be reached on (571) 272-3155. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

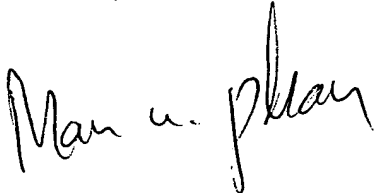
Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571) 272-2600.

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10. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have any questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at toll free 1-866-217-9197.

Mphan

June 21, 2005

A handwritten signature in cursive script that reads "Man u. phan".

MAN U. PHAN
PRIMARY EXAMINER